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DATA SHEET

74LV574

Octal D-type flip-flop;
positive edge-trigger (3-State)

Product specification
Supersedes data of 1997 Feb 03
IC24 Data Handbook

1998 Jun 10

Philips
Semiconductors

PHILIPS

Octal D-type flip-flop; positive edge-trigger (3-State) 74LV574

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Common 3-State output enable input
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV574 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT574.

The 74LV574 is an octal D-type flip–flop featuring separate D-type inputs for each flip-flop and non-inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	C_L = 15pF V_{CC} = 3.3V	13	ns
f_{max}	Maximum clock frequency	C_L = 15pF, V_{CC} = 3.3V	77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1 and 2	25	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	–40°C to +125°C	74LV574 N	74LV574 N	SOT146-1
20-Pin Plastic SO	–40°C to +125°C	74LV574 D	74LV574 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +125°C	74LV574 DB	74LV574 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV574 PW	74LV574PW DH	SOT360-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enabled input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0–D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0–Q7	3-State flip-flop outputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered)
20	VCC	Positive supply voltage

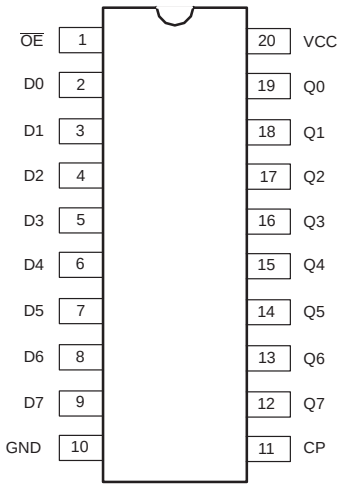
FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	Dn		Q0 to Q7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = High impedance OFF-state
↑ = LOW–to–HIGH clock transition

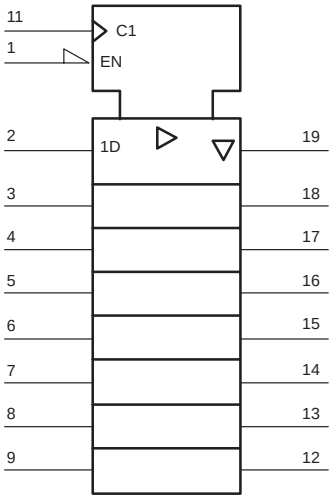
Octal D-type flip-flop; positive edge-trigger (3-State) 74LV574

PIN CONFIGURATION



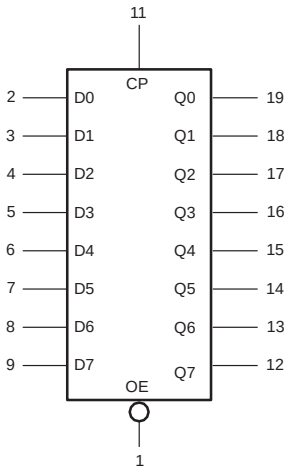
SV00714

LOGIC SYMBOL (IEEE/IEC)



SV00716

LOGIC SYMBOL



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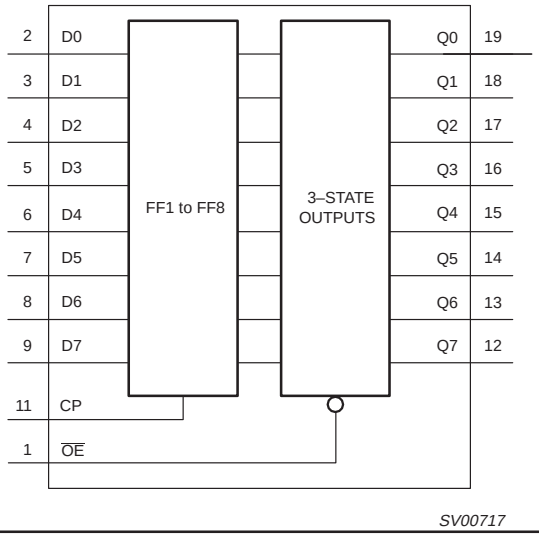
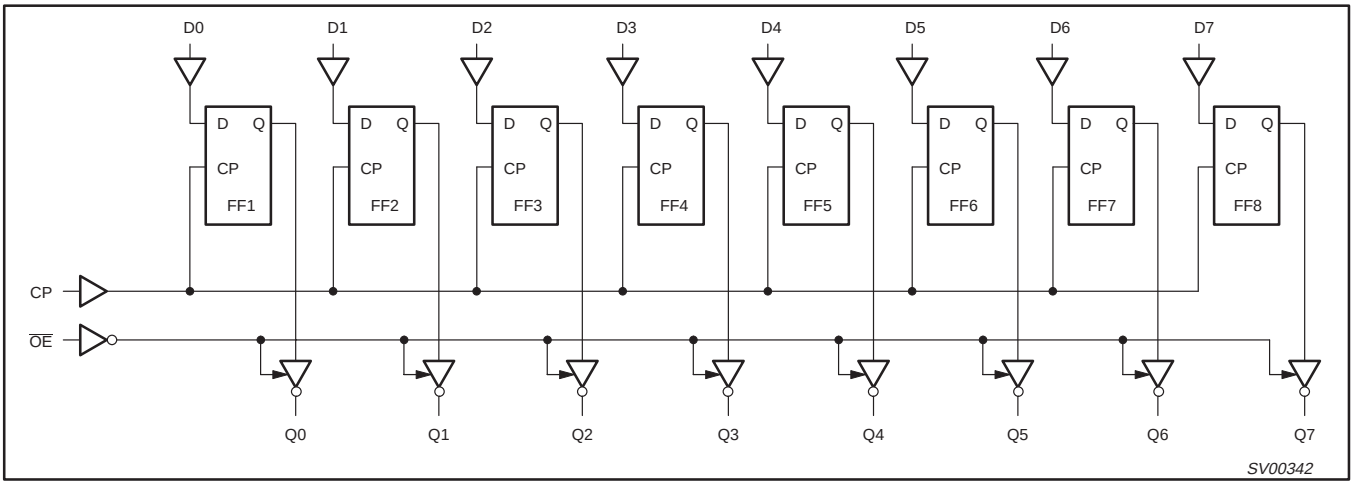
FUNCTIONAL DIAGRAM



SV00717

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < –0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < –0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$–0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note[1]	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTES:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V;V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 100µA	4.3	4.5		4.3		
	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V;V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 8mA	2.40	2.82		2.20		
		V_{CC} = 4.5V;V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 16mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or $V_{IL;}$ I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or $V_{IL;}$ I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or $V_{IL;}$ I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V;V_I = V_{IH} or $V_{IL;}$ I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V;V_I = V_{IH} or $V_{IL;}$ I_O = 100µA		0	0.2		0.2	
	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V;V_I = V_{IH} or $V_{IL;}$ I_O = 8mA		0.20	0.40		0.50	
		V_{CC} = 4.5V;V_I = V_{IH} or $V_{IL;}$ I_O = 16mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 5.5V; V_I = V_{IH} or $V_{IL;}$ V_O = V_{CC} or GND			5		10	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	Figure 1, 4	1.2	–	80	–	–	–	ns
			2.0	–	27	34	–	43	
			2.7	–	20	25	–	31	
			3.0 to 3.6	–	15[2]	20	–	25	
			4.5 to 5.5	–	–	17	–	21	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to Qn	Figure 2, 4	1.2	–	70	–	–	–	ns
			2.0	–	24	34	–	43	
			2.7	–	18	25	–	31	
			3.0 to 3.6	–	13[2]	20	–	25	
			4.5 to 5.5	–	–	17	–	21	
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$ to Qn	Figure 2, 4	1.2	–	75	–	–	–	ns
			2.0	–	27	27	–	34	
			2.7	–	21	21	–	26	
			3.0 to 3.6	–	16[2]	17	–	21	
			4.5 to 5.5	–	–	15	–	18	
t_W	Clock pulse width HIGH or LOW	Figure 1	2.0	34	9	–	41	–	ns
			2.7	25	6	–	30	–	
			3.0 to 3.6	20	5[2]	–	24	–	
t_{su}	Set-up time Dn to CP	Figure 3	1.2	–	10	–	–	–	ns
			2.0	22	4	–	26	–	
			2.7	16	3	–	19	–	
			3.0 to 3.6	13	2[2]	–	15	–	
t_h	Hold time Dn to CP	Figure 3	1.2	–	–10	–	–	–	ns
			2.0	5	–4	–	5	–	
			2.7	5	–3	–	5	–	
			3.0 to 3.6	5	–2[2]	–	5	–	
f_{max}	Maximum clock pulse frequency	Figure 1	2.0	15	40	–	12	–	MHz
			2.7	19	58	–	16	–	
			3.0 to 3.6	24	70[2]	–	20	–	

NOTE:

1. Unless otherwise stated, all typical values are at $T_{amb} = 25°C$.
2. Typical value measured at $V_{CC} = 3.3$V.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V and $\leq$ 3.6V
V_M = 0.5 * V_{CC} at V_{CC} < 2.7V and $\geq$ 4.5V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V and $\leq$ 3.6V
$V_X = V_{OL}$ + 0.1V_{CC} at V_{CC} < 2.7V and $\geq$ 4.5V
$V_Y = V_{OH}$ – 0.3V at $V_{CC} \geq$ 2.7V and $\leq$ 3.6V
$V_Y = V_{OH}$ – 0.1V_{CC} at V_{CC} < 2.7V and $\geq$ 4.5V

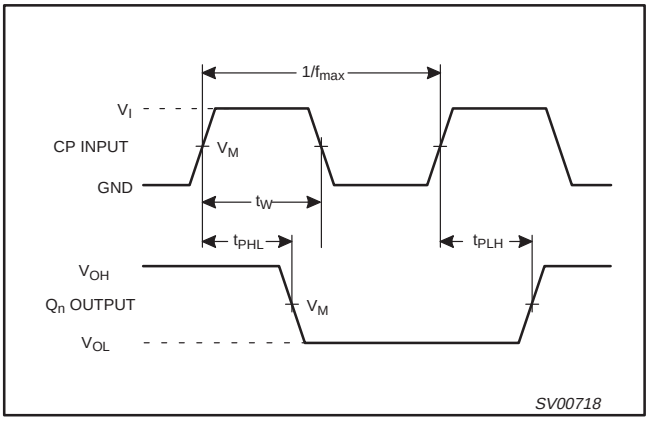


Figure 1. Clock (CP) to output (Qn) propagation delays, the clock pulse (CP) and the maximum clock pulse frequency

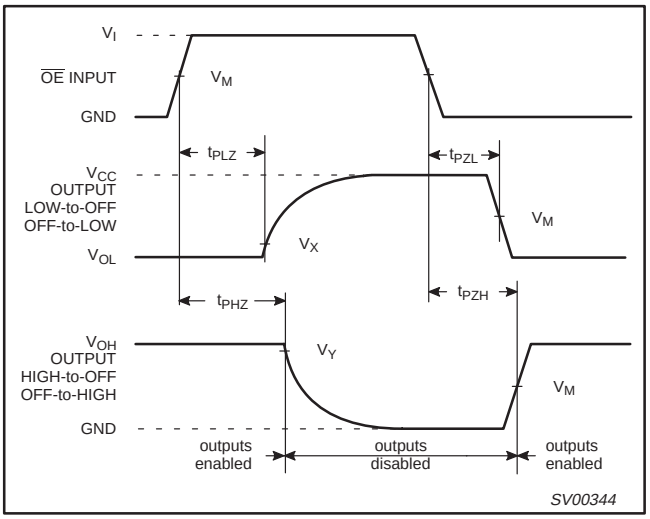


Figure 2. 3-state enable and disable times

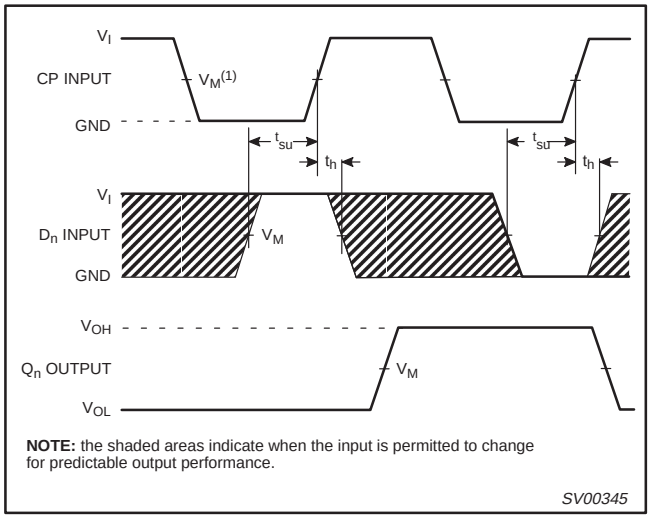
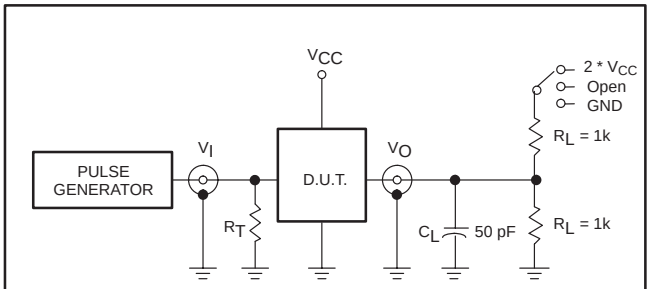


Figure 3. Data set-up and hold times for the Dn input to the CP input

NOTE:
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS
R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitiance.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

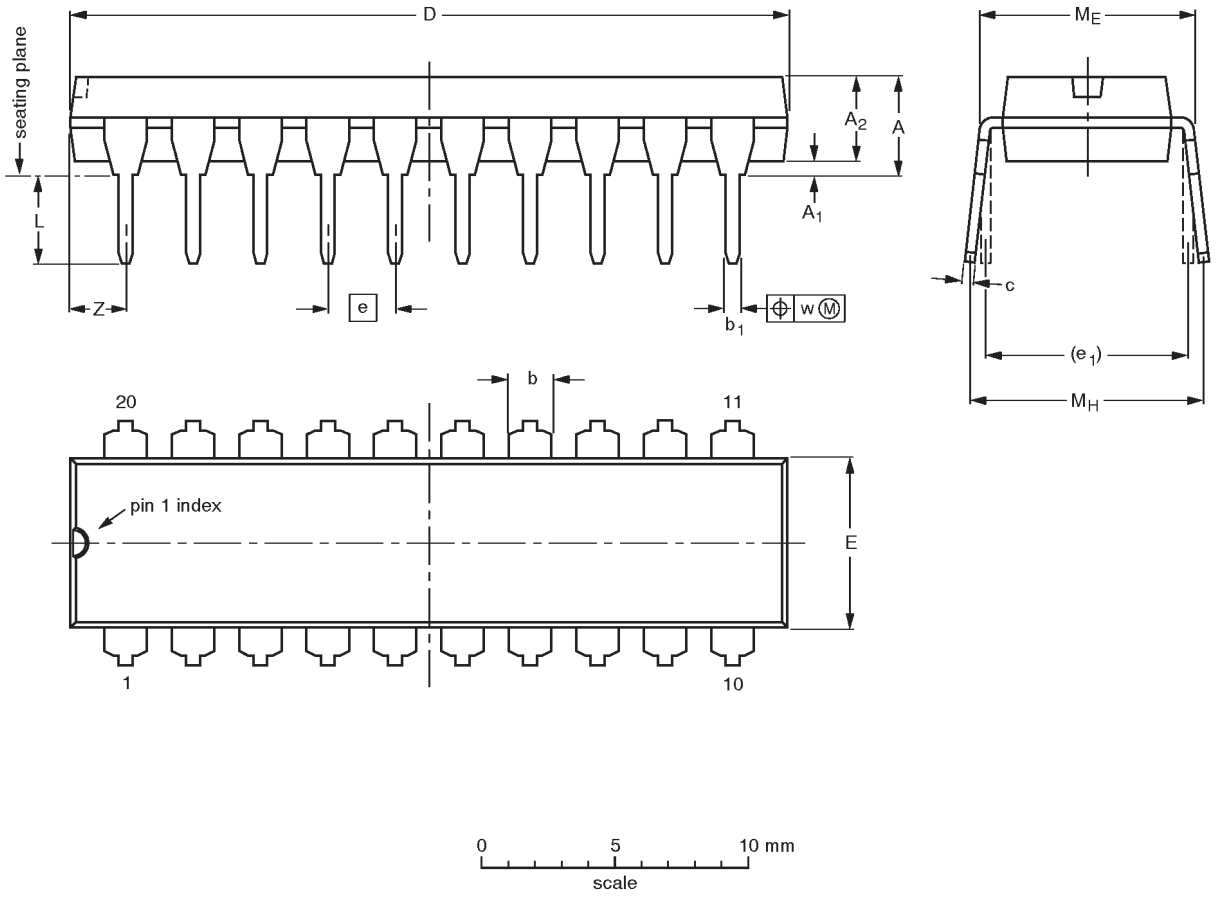
TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
$\geq$ 4.5V	V_{CC}

SV00896

Figure 4. Load circuitry for switching times

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

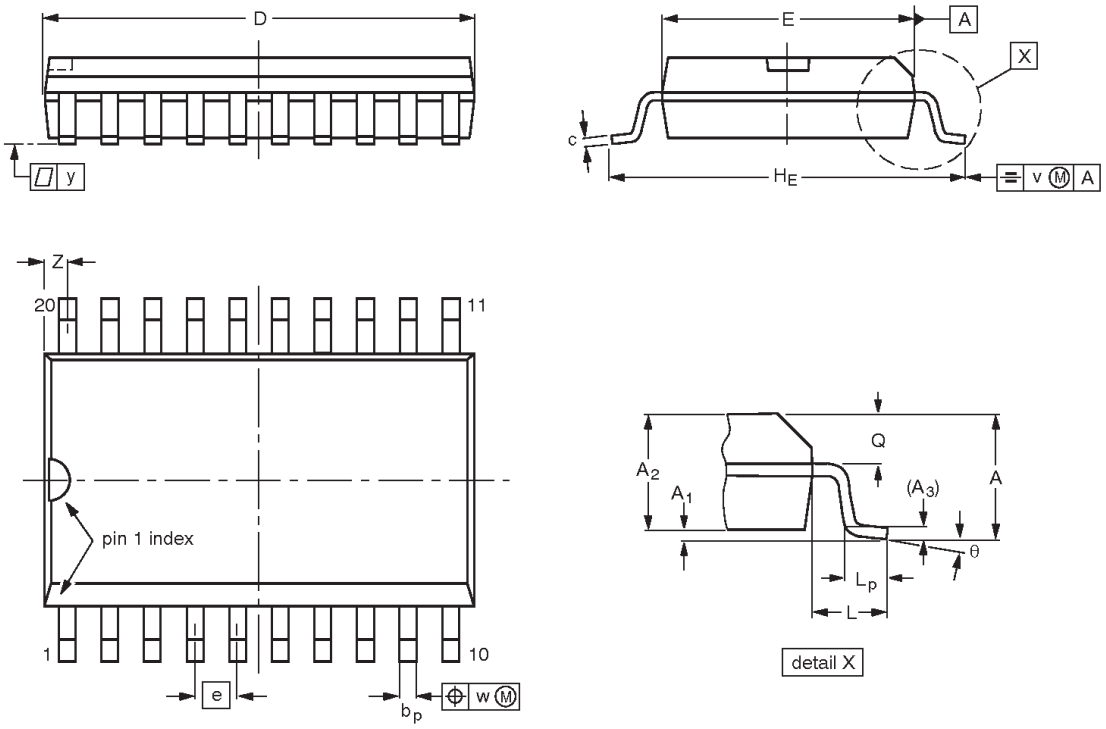
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

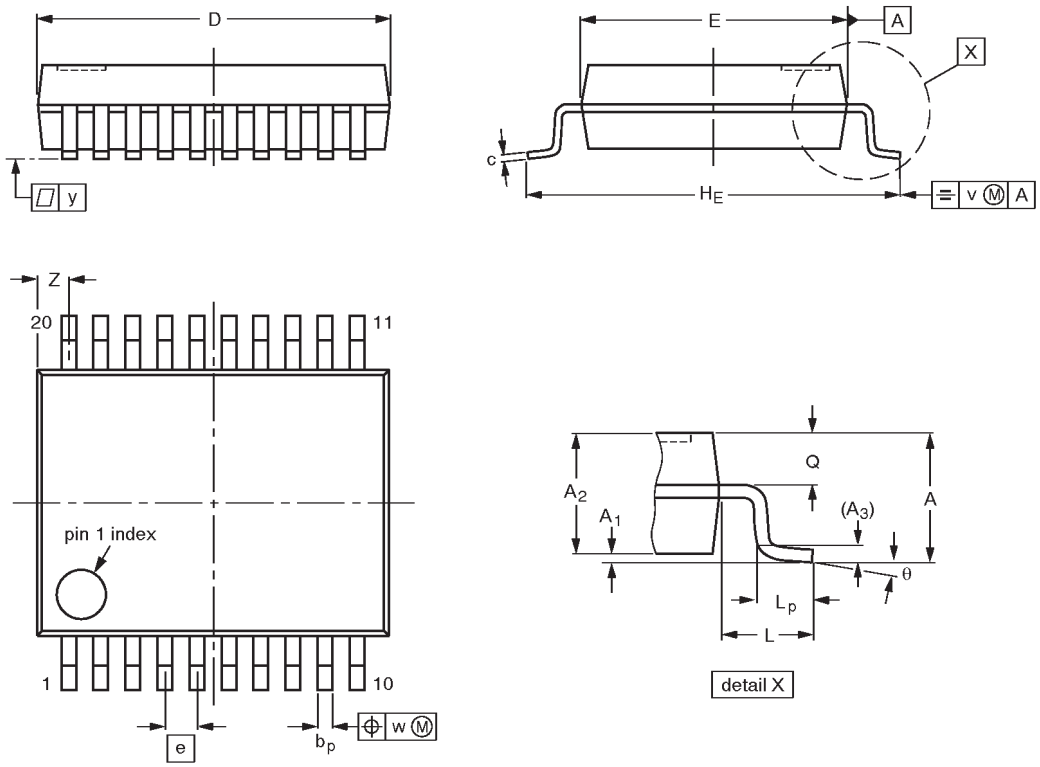
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

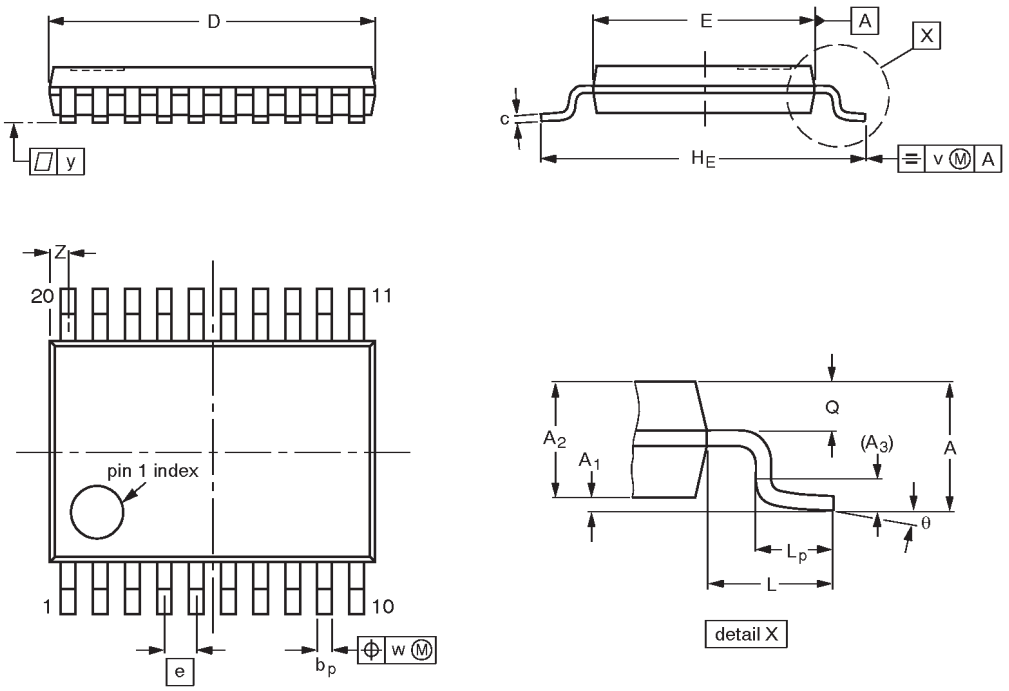
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

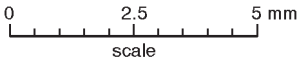
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04

DEFINITIONS

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